STATUS OF THE CLAIMS

The status of the claims of the present application stands as follows:

Claim 1-16: **(Cancelcd)**

17. **(Currently amended)** A device, comprising:

~~a)~~ an integrated circuit formed on a substrate and comprising a plurality of FETs wherein at least some of said plurality of FETs are finFETs each comprising:

~~i)~~ a) a fin having a source portion, a drain portion and a channel portion extending between said source portion and said drain portion, ~~each of said source portion and said drain portion having an upper surface and a length extending away from said channel portion~~ said fin having a base portion attached to said substrate;

~~a gate located at said channel portion so as to define a first reentrant corner between said upper surface of said source portion and said gate and a second reentrant corner between said upper surface of said drain portion and said gate~~; and

b) a first spacer ~~proximate said first reentrant corner and second spacer proximate said second reentrant corner, said first spacer extending a distance away from said gate in a direction along said source portion less than said length of said source portion and said second spacer extending a distance away from said gate in a direction along said drain portion a distance less than said length of said drain portion~~formed adjacent said base portion.

18. **(Currently amended)** A device according to claim ~~17~~19, further comprising a first hardmask remnant located between said ~~first~~ second spacer and said upper surface of said source and a second hardmask remnant located between said ~~second~~ third spacer and said upper surface of said drain.

19. **(Currently amended)** A device according to claim 17, wherein ~~said fin has a base portion attached to said substrate, said substrate including an undercut region located beneath at least a portion of said fin, said finFET further comprising a third spacer formed adjacent said base portion, said undercut portion containing at least a portion of said third spacer~~each of said source portion and said drain portion includes an upper surface having a width perpendicular to said length, each of said finFETs further comprising:

a) a gate located at said channel portion;

b) a first reentrant corner between said upper surface of said source portion and said gate;

c) a second reentrant corner between said upper surface of said drain portion and said gate;

d) a second spacer proximate said first reentrant corner and having a length extending along said gate substantially equal to said width of said source portion; and

e) a third spacer proximate said second reentrant corner and having a length extending along said gate substantially equal to said width of said drain portion.

20. **(Currently amended)** A device according to claim 17, wherein ~~each of~~ said first ~~and second~~ spacer comprises silicon dioxide.

21. **(New)** A device according to claim 17, wherein said substrate comprises an undercut region beneath at least a portion of said fin, said undercut region containing at least a portion of said first spacer.

22. **(New)** An integrated circuit comprising:

a) a substrate; and

b) a plurality of FETs formed on said substrate, wherein at least some of said plurality of FETs are finFETs each comprising:

i) a fin having a source portion, a drain portion and a channel portion extending between said source portion and said drain portion, said fin having a base portion attached to said substrate; and

ii) a first spacer formed adjacent said base portion.

23. **(New)** An integrated circuit according to claim 22, wherein each of said source portion and said drain portion includes an upper surface having a width perpendicular to said length, each of said finFETs further comprising:

a) a gate located at said channel portion;

b) a first reentrant corner between said upper surface of said source portion and said gate;

c) a second reentrant corner between said upper surface of said drain portion and said gate;

d) a second spacer proximate said first reentrant corner and having a length extending along said gate substantially equal to said width of said source portion; and

c) a third spacer proximate said second reentrant corner and having a length extending along said gate substantially equal to said width of said drain portion.

24. **(New)** An integrated circuit according to claim 23, further comprising a first hardmask remnant located between said second spacer and said upper surface of said source and a second hardmask remnant located between said third spacer and said upper surface of said drain.

25. **(New)** An integrated circuit according to claim 22, wherein said first spacer comprises silicon dioxide.

26. **(New)** An integrated circuit according to claim 22, wherein said substrate comprises an undercut region beneath at least a portion of said fin, said undercut region containing at least a portion of said first spacer.

27. **(New)** A finFET formed on a substrate, comprising:
   a) a fin having a source portion, a drain portion and a channel portion extending between said source portion and said drain portion, said fin having a base portion attached to the substrate; and
   b) a first spacer formed adjacent said base portion.

28. **(New)** A finFET according to claim 27, wherein each of said source portion and said drain portion includes an upper surface having a width perpendicular to said length, the finFET further comprising:
   a) a gate located at said channel portion;
   b) a first reentrant corner between said upper surface of said source portion and said gate;
   c) a second reentrant corner between said upper surface of said drain portion and said gate;
   d) a second spacer proximate said first reentrant corner and having a length extending along said gate substantially equal to said width of said source portion; and
   e) a third spacer proximate said second reentrant corner and having a length extending along said gate substantially equal to said width of said drain portion.

29. **(New)** A finFET according to claim 28, further comprising a first hardmask remnant located between said second spacer and said upper surface of said source and a second hardmask remnant located between said third spacer and said upper surface of said drain.

30. **(New)** A finFET according to claim 27, wherein said first spacer comprises silicon dioxide.

31. **(New)** A finFET according to claim 27, wherein the substrate comprises an undercut region beneath at least a portion of said fin, the undercut region containing at least a portion of said first spacer.

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